in the claims

Please amend the claims as follows:

Claims 1-28 (Canceled).

Claim 29 (Currently Amended): A semiconductor chip comprising:

a base substrate;

a ~~bulk device region having a bulk growth~~ single crystal layer epitaxially grown on a part of the base substrate~~, the bulk device region~~ having a first device-fabrication surface in which a bulk device is positioned ~~on the bulk growth layer~~;

a pn junction formed in the ~~bulk device region~~ single crystal layer and positioned above an interface between the base substrate and the ~~bulk growth~~ single crystal layer;

an SOI device region having a buried insulator on the other part of the base substrate and an SOI layer on the buried insulator, the SOI device region having a second device-fabrication surface in which an SOI device is positioned on the SOI layer, the first and second device-fabrication surface being positioned at a substantially uniform level;

a first isolation formed in the ~~bulk device region~~ single crystal layer so as to separate the bulk device, and a second isolation in the SOI device region so as to separate the SOI device, the first and second isolations being substantially the same depth and having a depth reaching the buried insulator; and

a boundary layer located at a boundary between the ~~bulk device region~~ single crystal layer and the SOI device region.

Claim 30 (Currently Amended): The semiconductor chip according to claim 29, wherein the ~~bulk growth~~ single crystal layer is a silicon ~~bulk growth~~ layer, and the boundary

layer reaches the base substrate and is made of one of polysilicon or silicon-based compound semiconductors.

Claim 31 (Previously Presented): The semiconductor chip according to claim 29, further comprising a third isolation positioned at the boundary and functioning at the boundary layer, wherein the first, second, and third isolations are of substantially the same depth.

Claim 32 (Currently Amended): ~~The~~ A semiconductor chip ~~according to claim 29~~, ~~further~~ comprising:

a base substrate;

a bulk device region having a bulk growth layer on a part of the base substrate, the bulk device region having a first device-fabrication surface in which a bulk device is positioned on the bulk growth layer;

a pn junction formed in the bulk device region and positioned above an interface between the base substrate and the bulk growth layer;

an SOI device region having a buried insulator on the other part of the base substrate and an SOI layer on the buried insulator, the SOI device region having a second device-fabrication surface in which an SOI device is positioned on the SOI layer, the first and second device-fabrication surface being positioned at a substantially uniform level;

a first isolation formed in the bulk device region so as to separate the bulk device, and a second isolation in the SOI device region so as to separate the SOI device, the first and second isolations being substantially the same depth and having a depth reaching the buried insulator;

a boundary layer located at a boundary between the bulk device region and the SOI device region; and

a dummy trench in the bulk device region between the bulk device and the SOI device.

Claim 33 (Previously Presented): The semiconductor chip according to claim 32, wherein the dummy trench is deeper than the buried insulator.

Claim 34 (Previously Presented): The semiconductor chip according to claim 32, wherein the bulk device positioned in the bulk device region includes a DRAM cell having a trench capacitor, and the dummy trench is a dummy capacitor.

Claim 35 (Previously Presented): A semiconductor chip comprising:

a base substrate;

a bulk device region having a bulk growth layer on a part of the base substrate, the bulk device region having a first device-fabrication surface in which a bulk device is positioned on the bulk growth layer;

an SOI device region having a buried insulator on the other part of the base substrate and an SOI layer on the buried insulator, the SOI device region having a second device-fabrication surface in which an SOI device is positioned on the SOI layer, the first and second device-fabrication surface being positioned at a substantially uniform level;

a boundary layer located at a boundary between the bulk device region and the SOI device region; and

a dummy trench formed in the bulk device region between the bulk device and the SOI device.

Claim 36 (Previously Presented): The semiconductor chip according to claim 35, wherein the dummy trench is a dummy capacitor.

Claim 37 (Previously Presented): The semiconductor chip according to claim 35, wherein the dummy trench is deeper than the buried insulator.

Claim 38 (Previously Presented): The semiconductor chip according to claim 35, wherein the bulk device positioned in the bulk device region includes a vertical bipolar transistor having an isolation trench, the isolation trench functioning as the dummy trench.

Claim 39 (Previously Presented): The semiconductor chip according to claim 35, wherein the bulk device positioned in the bulk device region includes a DRAM cell having a trench capacitor.

Claim 40 (Previously Presented): The semiconductor chip according to claim 35, wherein the bulk device positioned in the bulk device region includes a DRAM cell having a trench capacitor and a MOSFET, wherein the MOSFET is positioned between the DRAM cell and the dummy trench.

Claim 41 (Previously Presented): The semiconductor chip according to claim 35, wherein the bulk growth layer is a silicon bulk growth layer, and the boundary layer reaches the base substrate and is made of one of polysilicon or silicon-based compound semiconductors.

Claim 42 (Previously Presented): The semiconductor chip according to claim 35, wherein the bulk device region includes a first isolation separating the bulk device, and the SOI device region includes a second isolation separating the SOI device, the first and second isolations being of substantially the same depth.

Claim 43 (Previously Presented): The semiconductor chip according to claim 42, wherein the first and second isolations have a depth reaching the buried insulator.

Claim 44 (Previously Presented): The semiconductor chip according to claim 43, wherein the bulk device region has a pn junction positioned above an interface between the base substrate and the bulk growth layer.

Claim 45 (Previously Presented): The semiconductor chip according to claim 35, further comprising a first isolation in the bulk device region, a second isolation in the SOI device region, and a third isolation positioned at the boundary and functioning as the boundary layer, wherein the first, second, and third isolations are of substantially the same depth.

Claim 46 (Previously Presented): The semiconductor chip according to claim 45, wherein the first, second, and third isolations are deeper than the buried insulator.

Claim 47 (Previously Presented): The semiconductor chip according to claim 46, wherein the third isolation has a sidewall that is in contact with the buried insulator.

Claim 48 (Previously Presented): The semiconductor chip according to claim 35, further comprising a first isolation in the bulk device region, a second isolation in the SOI device region, and a third isolation positioned at the boundary and functioning as the boundary layer, wherein the second isolation is shallower than the third isolation.